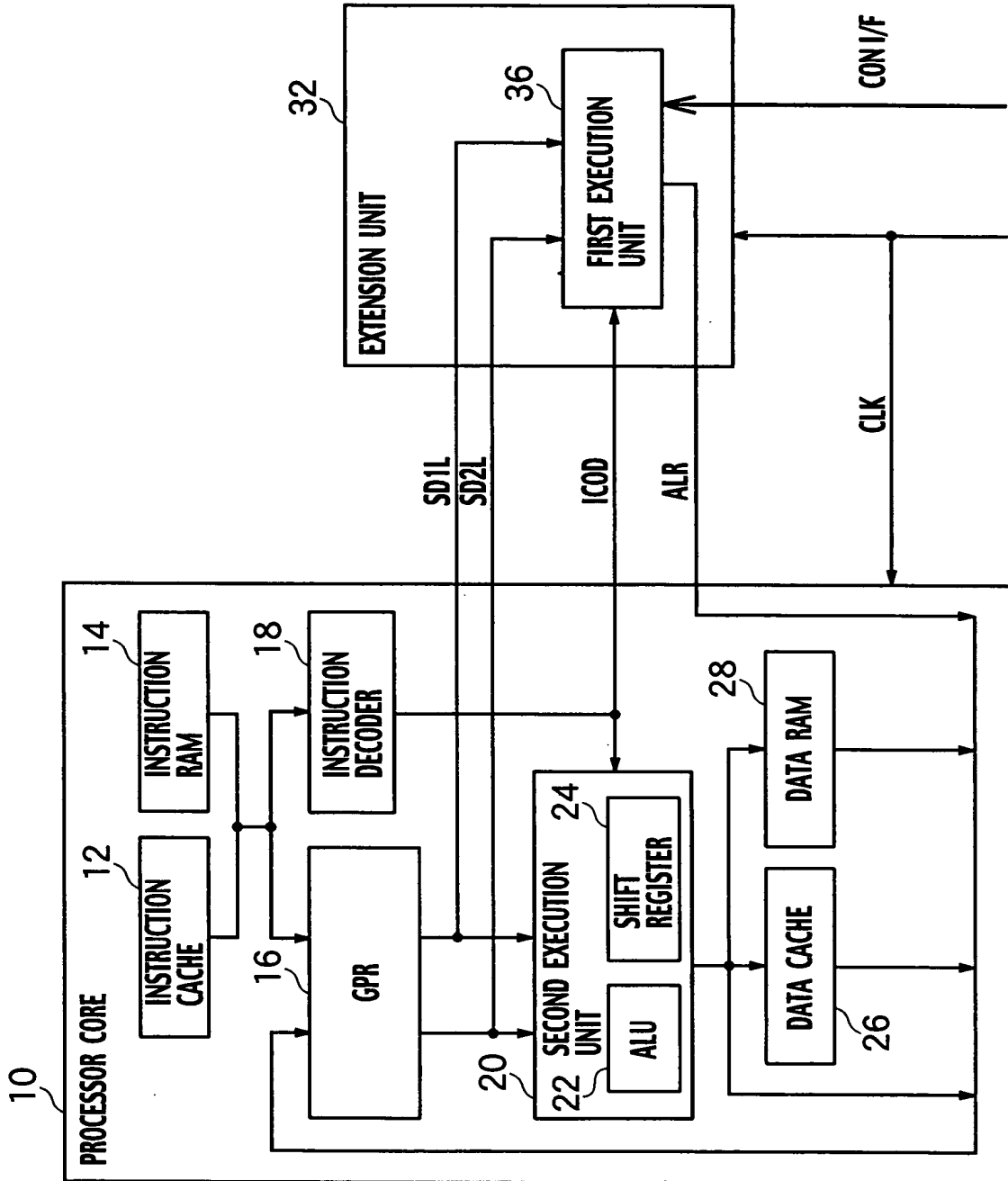


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FIG. 1





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FIG. 3

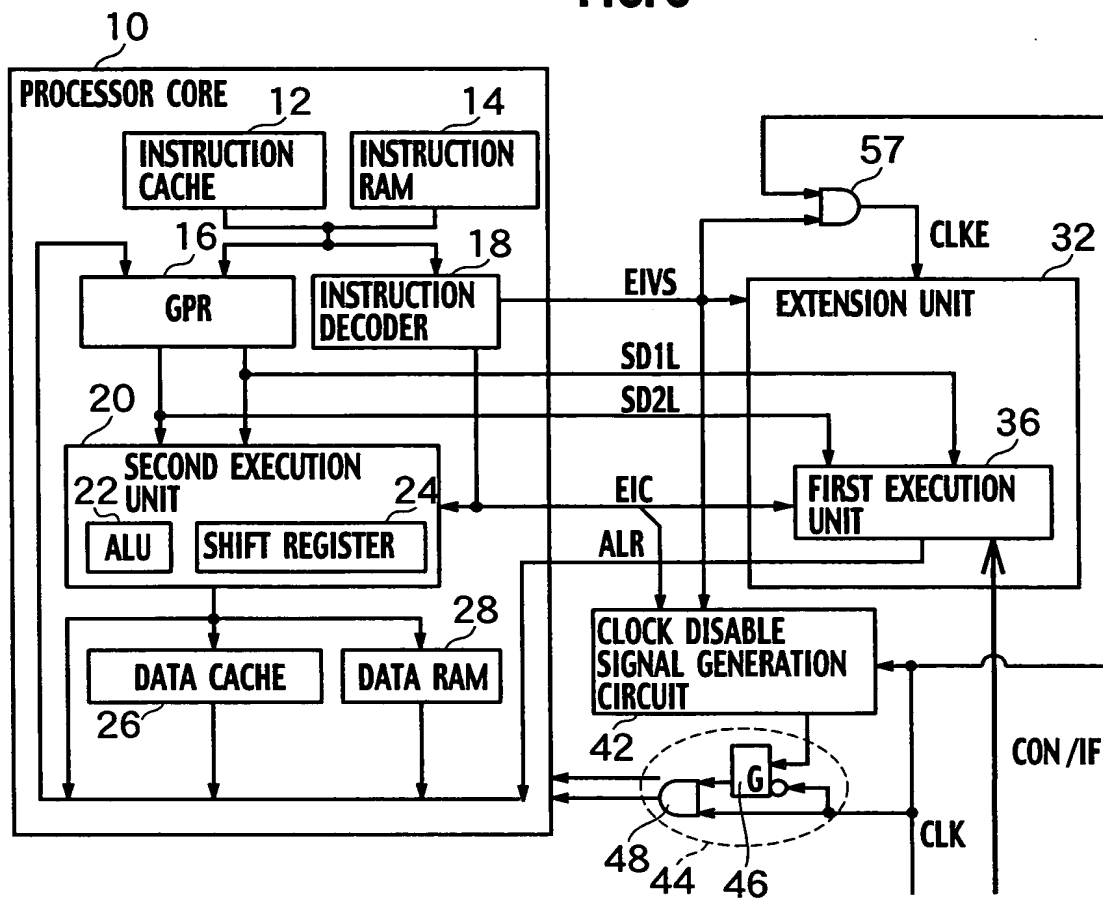
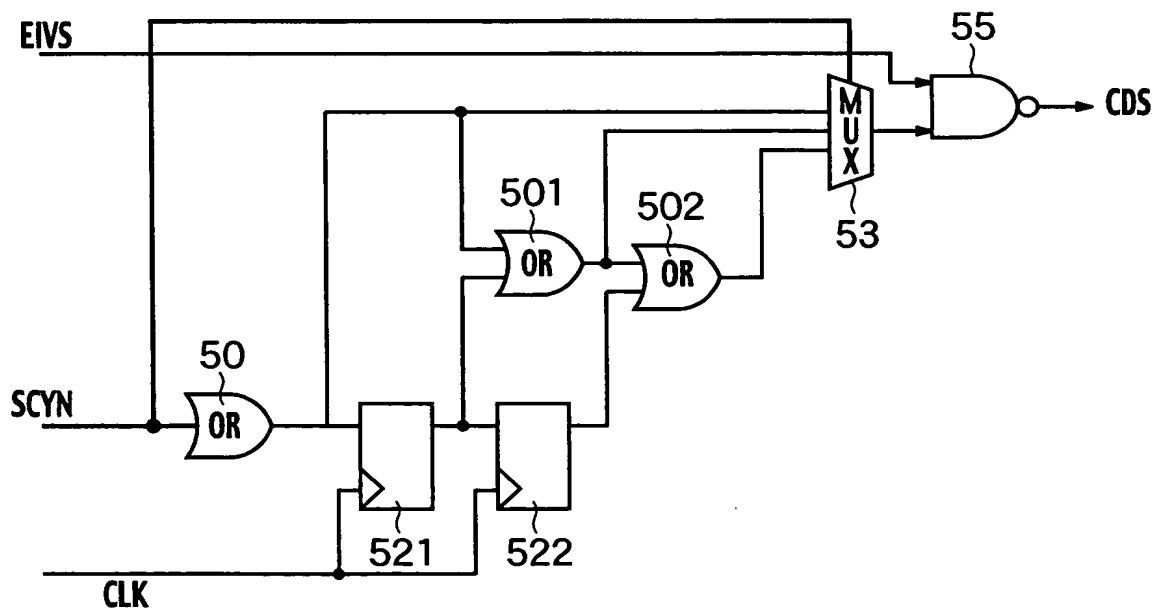


FIG. 4



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FIG. 5

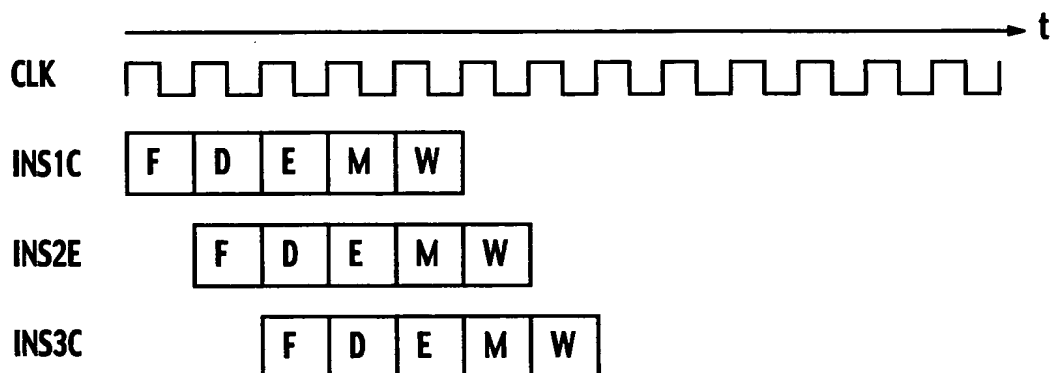
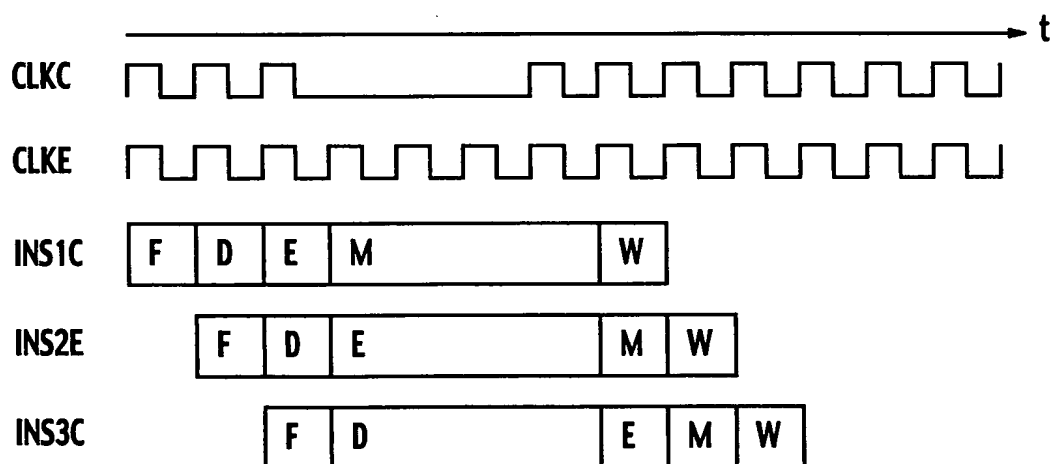
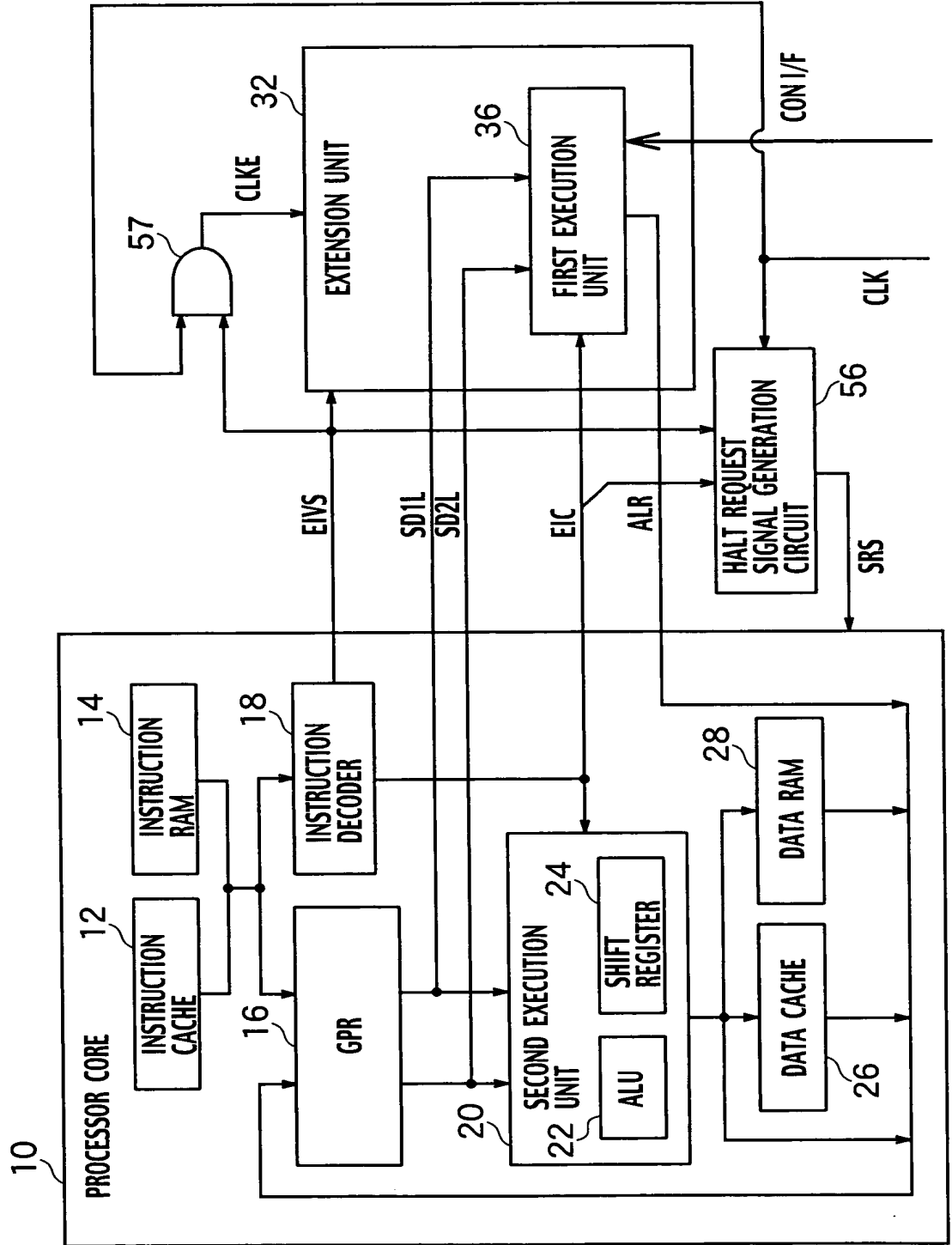


FIG. 6



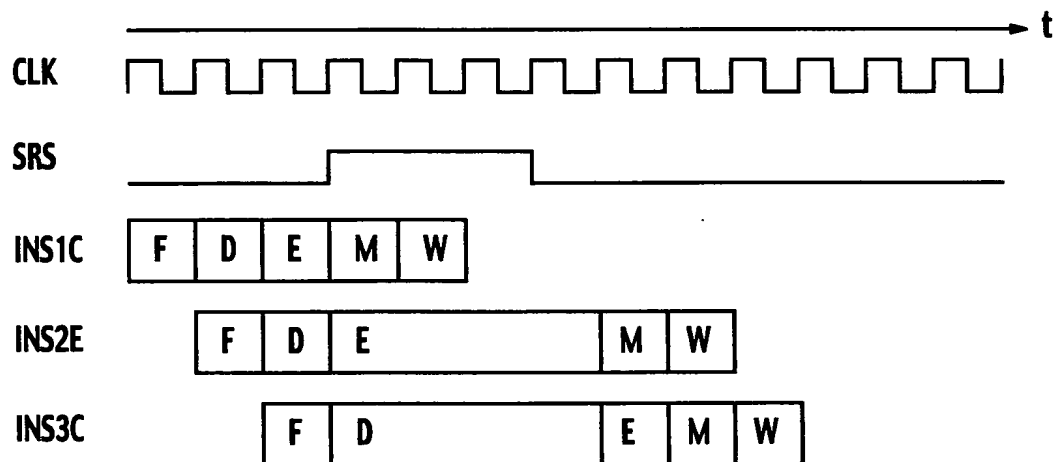
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FIG. 7

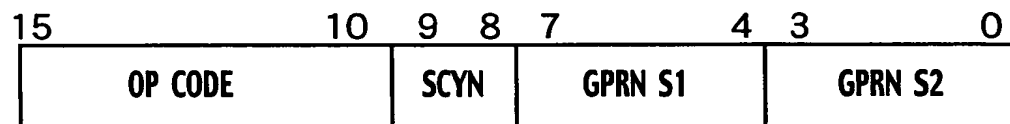


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**FIG. 8**



**FIG. 9**



The diagram illustrates a processor core 10, which is divided into two main functional blocks: a **PROCESSOR CORE** (12) and an **EXTENSION UNIT** (32).

**PROCESSOR CORE (12):**

- Instruction Path:** Includes an **INSTRUCTION CACHE** (14) and **INSTRUCTION RAM** (16). The **INSTRUCTION DECODER** (18) receives instructions from the cache and RAM, outputting **EIC** (Instruction Cache Hit/Valid) and **SD1L** (Source Data 1 Low) signals.
- Execution Path:** Features a **GPR** (General Purpose Register) (20) and a **SECOND EXECUTION UNIT** (22). The **SECOND EXECUTION UNIT** contains an **ALU** (Arithmetic Logic Unit) and a **SHIFT REGISTER** (24). It receives **SD2L** (Source Data 2 Low) and **CS** (Control Signal) signals.
- Data Path:** Includes a **DATA CACHE** (26) and **DATA RAM** (28). The **DATA CACHE** is connected to the **SECOND EXECUTION UNIT** and the **DATA RAM**. The **DATA RAM** is connected to the **DATA CACHE** and the **EXTENSION UNIT** via a **DR I/F** (Data Register Interface).

**EXTENSION UNIT (32):**

- Instruction Decoder:** An **INSTRUCTION DECODER** (34) receives **EAL I/F** (External Address/Local Interface) signals and outputs **SD1L** and **SD2L** signals to the processor core.
- Control and Memory:** Includes a **CONTROL REGISTER** (38) and **LOCAL MEMORY** (40). The **CONTROL REGISTER** is connected to the **INSTRUCTION DECODER** and the **RECONFIGURABLE FIRST EXECUTION UNIT**.
- Reconfigurable First Execution Unit:** This unit receives **ALR** (Address/Local Register) signals and is connected to the **LOCAL MEMORY** and the **DATA RAM** via the **DR I/F**.

**External Interfaces:**

- PB I/F** (Peripheral Bus Interface): Connects the processor core to the external bus.
- CON I/F** (Control Interface): Connects the extension unit to the external bus.
- LDB** (Local Data Bus): Connects the data cache and data RAM to the external bus.
- DR I/F** (Data Register Interface): Connects the data RAM to the extension unit.
- CS** (Control Signal): Connects the instruction decoder to the second execution unit.
- SD1L** and **SD2L** (Source Data 1 Low and 2 Low): Connect the instruction decoder to the GPR and second execution unit.
- EIC** (Instruction Cache Hit/Valid): Connects the instruction decoder to the instruction cache.
- EAL I/F** (External Address/Local Interface): Connects the extension unit to the external bus.
- ALR** (Address/Local Register): Connects the extension unit to the data RAM.

FIG. 11

